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FOR

# MEMORY DEVICE PACKAGING INCLUDING STACKED PASSIVE DEVICES AND METHOD FOR MAKING THE SAME

Inventor(s): Eleanor P. Rabadam
Charles A. Lopez
Richard B. Foehringer

Prepared by: Kenneth M. Seddon,
Senior Patent Attorney

intel®
Intel Corporation
5000 W. Chandler Blvd., CH6-404
Chandler, AZ 85226-3699
Phone: (480) 554-9732
Facsimile: (480) 554-7738

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# MEMORY DEVICE PACKAGING INCLUDING STACKED PASSIVE DEVICES AND METHOD FOR MAKING THE SAME

## BACKGROUND

Memory devices such as, for example, non-volatile memory devices often involve the use of programming/erasing voltage potentials that are typically different that the normal operating voltage potentials. As a result, the memory devices may be connected to additional circuitry that generates and regulates the voltage potentials used to program or erase the memory device. However, the additional circuitry may increase the cost associated with the memory devices. The additional circuits and components may also affect the reliability of the memory device as there as more components involved whose failures may result in a failure of the operation of the memory.

Thus, there is a continuing need for better ways to package memory devices.

## BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features, and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

The sole figure is an enlarged cross-sectional view of a package for an integrated circuit in accordance with an embodiment of the present invention.

It will be appreciated that for simplicity and clarity of illustration, elements illustrated in the figure have not necessarily been drawn to scale. For example, the dimensions of some of the elements are exaggerated relative to other elements for clarity.

## DETAILED DESCRIPTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present invention.

In the following description and claims, the terms "coupled" and "connected," along with their derivatives, may be used. It should be understood that these terms are not intended as synonyms for each other. Rather, in particular embodiments, "connected" may be used to indicate that two or more elements are in direct physical or electrical contact with each other. "Coupled" may mean that two or more elements are in direct physical or electrical contact. However, "coupled" may also mean that two or more elements are not in direct contact with each other, but yet still co-operate or interact with each other.

Turning to FIG. 1, an embodiment 100 in accordance with the present invention

is described. A ball grid array (BGA) package 10 may include a substrate 12 that may be electrically coupled to external circuitry using a multiplicity of solder balls 25. It should be understood that the scope of the present invention is not limited to BGA packages, as other packages may be alternatively used.

Package 10 may contain an integrated circuit die 14 attached to the substrate 12, for example using a suitable adhesive 16. Adhesive 16 may comprise a non-conductive material so as to provide electrical isolation between substrate 12 and integrated circuit die 14. Alternatively, adhesive 16 may comprise a conductive material so as to electrically couple integrated circuit 14 to substrate 12 or the underlying solder balls 25.

Although the scope of the present invention is not limited in this respect, integrated circuit die 14 may include a non-volatile memory array such as an electrically programmable read-only memory (EPROM), electrically erasable and programmable read only memory (EEPROM), single-bit flash memory, multi-bit flash memory, etc.

In one embodiment, all or a portion of a voltage regulator circuit may be formed within package 10. The voltage regulator may be used to provide voltage potentials to be used during the operation of integrated circuit die 14. For example, although the scope of the present invention is not limited in this respect, the voltage regulator may provide voltage potentials to program and/or erase the non-volatile memory within integrated circuit die 14.

Although the scope of the present invention is not limited in this respect passive components 60 and 61 may be formed and molded within package 10. For example

passive components 60 and 61 may include components such as capacitors, inductors, resistive elements, or other integrated components associated with charge pump circuitry, voltage regulator circuitry, etc. Although this list is not meant to be exhaustive as any active or passive device may be molded in package 10 if desired.

Passive components 60-61 may be mounted or attached to the upper surface of integrated circuit die 14, for example using an adhesive 18. Adhesive may comprise a non-conductive material such as, for example, an epoxy so as to provide electrical isolation between passive components 60 and 61. Although the scope of the present invention is not limited in this respect, for in alternative embodiments, adhesive 18 may comprise some conductive material (e.g. solder paste or conductive epoxy) so as to electrically couple passive components 60-61 to integrated circuit die 14. The thickness of adhesive layer may be varied as desired, but may be less than about 0.050 millimeters so as to reduce the overall thickness of package 10.

Wire bonds 20 may be formed between passive components 60-61 and substrate 12, or between integrated circuit die 14 and substrate 12 as shown in FIG. 1. Alternatively, or in addition to, wire bonds may be formed between passive components 60-61 and integrated circuit die 14. Wire bonds 20 may provide electrical connection to integrated circuit die 14, substrate 12 and/or any of the underlying solder balls 25.

Thereafter, integrated circuit die 14 and passive components 60-61 may be molded in a non-conductive encapsulant 24 to form a molded array package (MAP), although the scope of the present invention is not limited in this respect. Although only a few passive components are shown in FIG. 1, it should be understood that in alternative embodiments just one or all the passive components associated with the

operation of integrated circuit die 14 may be included within package 10. In addition, it should be understood that the scope of the present invention is not limited in application to only non-volatile memory devices, or only to memory devices in general.

Accordingly, the embodiment illustrated in the figure demonstrates a power supply in package (PSIP) arrangement where at least portions of the circuitry or components associated with the operation of integrated circuit die 14 may be mounted or stacked on upper surface of integrated circuit die 14 and within package 10. Package 10 may substantially maintain the form factor of corresponding non-PSIP packages (e.g. separate packages for the memory device, for the passive components, and for the voltage regulator) so that package 10 may fit within the space allocated on boards for corresponding non-PSIP packages that perform substantially the same features. As a result, a compact package 10 may be achieved that has lower manufacturing costs while substantially maintaining the form factor of corresponding (but more expensive) non-PSIP packages.

While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

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